REMARKS

Claims 1-31 will be pending upon entry of the present amendment. Claims 1-10, 12-18, 20, 22, and 24 are currently amended. New independent claim 28 and new dependent claims 25-27 and 29-31 have been added. No new matter has been added to the application. The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

One embodiment of the present invention is a device that translates instructions belonging to a pipelined scalar processor, an ARM RISC processor for example, into instructions belonging to a very large instruction word (VLIW) processor, an LX processor for example. In such an embodiment, the inventors have considered the significant differences between architectures of pipelined scalar processors and VLIW processors and have discovered operations that maximize efficiency when performing translations. As one example of such a discovery, an embodiment of the present application performs static translations of pipelined scalar processor instructions, thus leaving the core of the VLIW processor unaltered. The static translations are then used dynamically, yielding a robust emulation of the scalar processor. The prior art clearly discloses no such feature, and instead, specifically teaches dynamic translation and dynamic use of the translations.

In contrast to the prior art, one embodiment of the present invention performs the translations by adding functional units to the VLIW processor, keeping the VLIW processor core unaltered, and performing translations in absence of direct access to the resources of the core. In one embodiment, for example, because only a minimal part of the ARM instruction set is directly compatible with the LX instruction set, and because the ARM processor has a variety of addressing and execution modes not found on the LX processor, trying to perform translations dynamically has immediate, detrimental effects in an emulation of an ARM processor on an LX processor (Pg. 15, lines 22-28, Pg. 16, lines 1-3). However, by performing the translation with a distinct functional unit such as a translational device (*E.g.*, performing said translation in the absence of direct access to resources of the core), the device avoids these detrimental effects.

The applicants further point out that this discussion of one embodiment does not limit the presented claims in any way, but is merely for the benefit of the Examiner.

1. Antecedent Basis

The applicants have amended claims 1-10, 12-18, 20, 22, and 24, to include proper antecedent basis and to more distinctly identify the allowable subject matter in the present application. The applicants wish to clarify that these amendments to claims 1-10, 12-18, 20, 22, and 24 17 are made for purposes of placing the claims in condition for allowance, and not in response to any rejections made based on cited art. The applicants submit that no substantive limitations have been added to the amended claims, and support for all amendments is included in the present specification. Therefore, no prosecution history estoppel should arise from these amendments.

2. Rejections Under 35 U.S.C. § 101

At paragraph 2 of the Office Action, claim 24 stands rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

In response to the rejection, claim 24 is amended herewith into a proper "computer-readable medium" format, and thus, amended claim 24 is directed to a tangible embodiment. Accordingly, amended claim 24 is directed to statutory subject matter and Applicants respectfully request withdrawal of the rejection to the claim.

3. Rejections Under 35 U.S.C. § 103(a)

In the Office Action, at paragraph 4, claims 1-16 and 19-24 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over *VanDyke* (U.S. Patent 6,934,832), hereinafter *Van Dyke*, in view of *Schlansker* (U.S. Patent 6,408,428). In subsequent paragraphs of the Office Action, the Examiner discusses claims 1-16 and 19-24 in view of *Van Dyke* and *Borrill* (U.S. Patent 6,496,922), hereinafter *Borrill*. The Examiner does not discuss *Schlansker* at all, so the applicants assume that the Examiner's rejection was intended to be based on *Van Dyke* and *Borrill* rather than *Schlansker*.

a. *Schlansker* is not on point

The applicants contend that the invention *Schlansker* discloses is far remote from the subject matter disclosed in the present claims in that it does not mention translations from a first set of instruction into instructions belonging to a second set of instructions; rather, *Schlansker* merely concerns the definition of the architecture and compiler of a VLIW processor.

b. The prior art does not teach translating pipelined scalar processor instructions to VLIW processor instructions

Van Dyke and *Borrill* do not teach or suggest the invention of claim 1, which recites translating pipelined scalar processor instructions to VLIW processor instructions. Specifically, *Van Dyke* concerns the translation of a complex non-pipelined scalar processor instruction set (*E.g.* x86) into a native instruction set for execution on multiple pipelines (col. 31, lines 64-67; col. 33, lines 22-24), and *Borrill* discloses translation of instructions from several instruction set families, such as VLIW, SPARC, PowerPC, x86, (col. 4, Table 1), into the VLIW instructions (col. 5, lines 19-21). It would be evident to one skilled in the art that the instructions of the instruction set families disclosed in *Van Dyke* and *Borrill* are not pipelined scalar processor instructions. So, even though *Borrill* discloses operation of native VLIW instructions on his processor (col. 3, lines 9-11), the combination of *Van Dyke* and *Borrill* still does not teach or suggest to one skilled in the art the translation of a set of pipelined scalar processor instructions into a set of VLIW processor instructions.

c. The prior art does not teach performing translations in the absence of direct access to resources of the VLIW processor core

Van Dyke and *Borrill* do not teach or suggest performing translations in the absence of direct access to resources of the VLIW processor core, as recited in claim 1. Instead, the prior art performs dynamic translations of instructions from one instruction set to another by directly accessing the resources of a VLIW core. More specifically, unlike claim 1, *Van Dyke* illustrates in Figure 1c that his functional units, the x86 aligner and the x86 converter 136, perform

translations in direct access to the resources of the core. Van Dyke expressly calls out "control on the converter 186" (col. 32, lines 53-58).

Additionally, *Borrill* discloses Dynamic Decode Units (DDU1 – DDU7 in Fig. 5), which dynamically translate instructions from several instruction sets (col. 4, Table 1) into VLIW instructions (col. 5, lines 19-21) using core resources. *Borrill's* device interrogates each instruction, one-by-one (Fig. 4, step 132) to determine which of the plurality of instructions set families it belongs to before performing the dynamic translation (col. 4, line 23-25). Unlike claim 1, *Borrill's* operations are not performed in absence of direct access to the said resources of the core.

For at least the foregoing reasons, claim 1 is nonobvious in view of the prior art, and further, because claims 2-19 depend from claim 1, claims 2-19 are also nonobvious.

Although the language of claims 20-24 are not identical to that of claim 1, the allowability of claims 20-24 will be apparent in view of the above remarks.

d. Claims 14, 15, and 16

Applicants respectfully submit that claims 14-16 are allowable even apart from their dependence on claim 1. Paragraph 12 of the Office Action suggests that *Borrill* teaches a set of control pointers in "table 1 (e.g., see col. 30 lines 5-62)." The applicants respectfully point out that *Borrill's* Table 1, shown in column 4, discloses codes and native processors; that *Borrill* does not have column 30; and that *Borrill* does not recite "pointers" in his patent. The applicants further point out that prior art *Van Dyke* similarly makes no such corresponding disclosures.

4. Acknowledgement of Allowed Claims and Allowable Subject Matter

Applicants appreciate the Examiner's indication that the subject matter of claims 17-18 is allowable. The applicants believe, however, that amended base claim 1 is also allowable as discussed above, and therefore claims 17 and 18 are not being placed in independent form.

a. Claim 27

The applicants further note that claim 27 has been added. The Examiner will note that claim 27 recites similar limitations to claim 17, however the applicants have changed the increment of the selected register from "a value four" to "a number equal to a length in bytes of each" instruction. Support for this limitation can be found on page 2 of the present specification, which discusses the degree of parallelism of the pipelined scalar processor instructions, and page 23 of the present application, which discusses incrementing the selected register. The applicants appreciate the time and courtesy of the Examiner in conducting a telephone interview with the undersigned attorney on May 11, 2006, during which time this amendment was discussed. The Examiner indicated that even in light of a new search, claim 17 would likely still contain allowable subject matter.

b. Claims 28-31

In further view of the Examiner's conclusion that the subject matter of claims 17-18 is allowable, the applicants have also created new independent claim 28 and new dependent claims 29-31. Independent claim 28 contains the elements of amended base claim 1 and intervening amended dependent claim 13 along with the subject matter from amended dependent claim 17, which the Examiner has indicated contains allowable subject matter. The applicants respectfully urge review by the Examiner and submit that claim 28 is in condition for allowance. Claims 29-31 depends from claim 28, and thus, claims 29-31 are similarly in condition for allowance.

5. New Claims 25 and 26

New claims 25 and 26 depend from claim 24, and thus, claims 25 and 26 are similarly in condition for allowance.

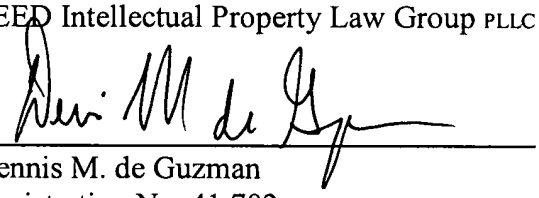
6. Conclusion

Applicants thank the Examiner for indicating the allowable subject matter of claims 17-18. In light of the above amendments and remarks, Applicants respectfully submit

that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that all pending claims 1-30 are allowable. Applicants, therefore, respectfully request that the Examiner reconsider this application and timely allow all pending claims. The Examiner is encouraged to contact Mr. Iannucci by telephone to discuss the above and any other distinctions between the claims and the applied references, if desired. If the Examiner notes any informalities in the claims, he is further encouraged to contact Mr. Iannucci by telephone to expediently correct such informalities.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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